IN THE CLAIMS

Please amend the claims as follows.

For the Examiner's convenience, a list of all claims is included below.

1-62 (Cancelled)

63. (Currently amended) A microelectronic structure comprising:

a substrate;

a gate electrode formed over the substrate and defining an underlying channel region in the substrate, said gate electrode having a barrier layer formed on a sidewall of the gate electrode to prohibit the silicidation of the sidewall;

a source/drain extension formed in the substrate adjacent the gate electrode and encroaching laterally into the underlying channel region a first distance, the source/drain extension having a first silicide layer formed therein, the first silicide encroaching laterally into the underlying channel region a second distance less than the first distance; and

a source/drain region formed in the substrate adjacent the source/drain extension and having an activated doped region with a second silicide layer disposed therein, both the activated doped region and the second silicide layer are aligned with a spacer disposed along sidewalls of the gate electrode such that both the activated doped region and the second silicide layer encroach laterally into the underlying channel region a third distance due to alignment with the spacer disposed along the sidewalls, the third distance less than the second distance, said source/drain extension having less dopant concentration than the activated doped region.

64. (Previously amended) The microelectronic structure of claim 63, wherein the activated doped region is thicker than the source/drain extension.

65. (Previously presented) The microelectronic structure of claim 63, wherein the second silicide layer is thicker than the first silicide layer.

66. (Previously presented) The microelectronic structure of claim 63, wherein the activated doped region and the source/drain extension comprise ion implanted material.

67. (Previously presented) The microelectronic structure of claim 63, wherein the first and second silicide layers comprises different metals.

68. (Previously presented) The microelectronic structure of claim 63, wherein the first and second silicide layers comprise a same metal.

69. (Previously presented) The microelectronic structure of claim 63, wherein the second silicide layer comprises $CoSi_2$.

70. (Previously presented) The microelectronic structure of claim 63, wherein the second silicide layer comprises $TiSi_2$.

71. (Previously presented) The microelectronic structure of claim 63, wherein the second silicide layer comprises nickel silicide.

72. (Previously presented) The microelectronic structure of claim 63, wherein the first silicide layer comprises $CoSi_2$.

73. (Previously presented) The microelectronic structure of claim 63, wherein the first silicide layer comprises $TiSi_2$.

74. (Previously presented) The microelectronic structure of claim 63, wherein the gate electrode has a third silicide layer formed on the top surface of the gate electrode.

75. (Previously presented) The microelectronic structure of claim 63, wherein the barrier layer comprises silicon nitride.

76-90 (Cancelled)